

Development of Noise Analysis Method for DC-DC Converter Circuit

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Abstract

In general, a DC-DC converter circuit which converts the voltage of battery mounted on vehicle is installed in ECU (Electronics Control Unit) for vehicle. As strong noise is generated over a wide band by switching operation of this circuit, it is very difficult to take EMC (Electro Magnetic Compatibility) measure. Therefore, the need of noise simulation analysis has become high in order to incorporate EMC design into the product design from the initial stage of ECU development.

However, general simulation analysis method cannot apply to actual ECU development in many cases because of problem of the accuracy and the time.

Therefore, we have developed an efficient simulation analysis method. By using this method, ECU development designer who is not an EMC specialist himself / herself can easily incorporate EMC design into the product design from the initial stage of design. We introduce this analysis method in this paper.

1. Introduction

The automobile industry is entering a once-in-a-century period of massive changes including autonomous driving and vehicle electrification. As a result, ECUs (Electronics Control Units) are becoming more sophisticated and complex. On the other hand, global EMC (Electro Magnetic Compatibility) laws and regulations are becoming stricter, and the environment surrounding ECUs is becoming harsher.

In general, an ECU converts power supplied from the battery installed in the vehicle into the voltage required for the operation of microcomputers and other instruments using a DC/DC converter circuit mounted on the ECU board. At that time, the switching operation results in powerful harmonic noise from low frequencies to broad-band ranges. Measures in product development for these EMC are normally implemented from the design stage. However, as it involves various design conditions such as one for the board, often it inevitably results in EMC measures from the product evaluation stage. In this case, there

are many various restrictions and a significant loss of time and cost are caused.

Therefore, there are many efforts around the world for the noise simulation analysis of DC/DC converters with the aim to include EMC design in the initial stage of design. Here, we describe our efforts to have developed a new efficient simulation analysis method for a DC/DC converter step-down circuit.

2. Operation and noise mechanism of DC/DC converter^{1), 2), 3)}

The role of a step-down DC/DC converter circuit is to split the input DC voltage by turning a switching element (MOS FET, etc.) on and off, and use a coil and capacitor to perform smoothing, thus outputting the desired DC voltage. For the output voltage, the switching regulator IC performs constant detection and the switching element is controlled to turn on or off to match the detected status, thus achieving a uniform voltage (**Fig. 1**).

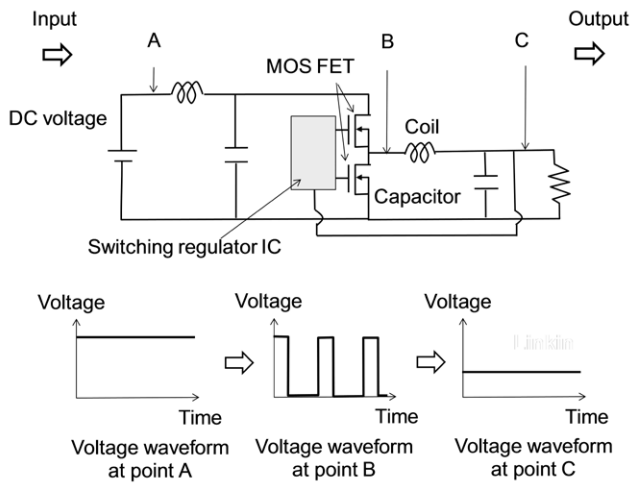


Fig. 1 Step-down DC/DC converter circuit and voltage waveform

Since, at this time, the switching frequency of the switching regulator IC ranges from several hundred kHz to several MHz, multiplied noise appears with short frequency intervals across the broad-band range around AM, FM, and DAB radio frequencies (510 kHz to 245 MHz) (Fig. 2).

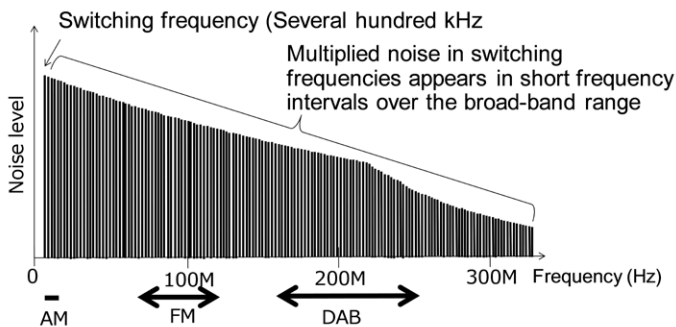


Fig. 2 Multiplied noise in switching frequencies

Also, during the rise of the switching node, a large ringing occurs (Fig. 3). Regarding this noise mechanism, when the TOP-side MOS FET (Qt) turns ON, the BOTTOM-side MOS FET (Qb) is charged with parasitic capacitance C (several pF to several tens of pF). Then, the energy stored in parasitic inductance L of the board wiring inside the loop (bold frame in Fig. 3) consisting of the input capacitor, Qt, and Qb causes resonance with parasitic capacitance C, which has smaller capacitance than the input condenser but controlling influence. At this time, harmonic noise across the board-band in the ringing frequency (around 100 M to 300 MHz) builds up and FM and DAB band noise may become a problem (Fig. 4).

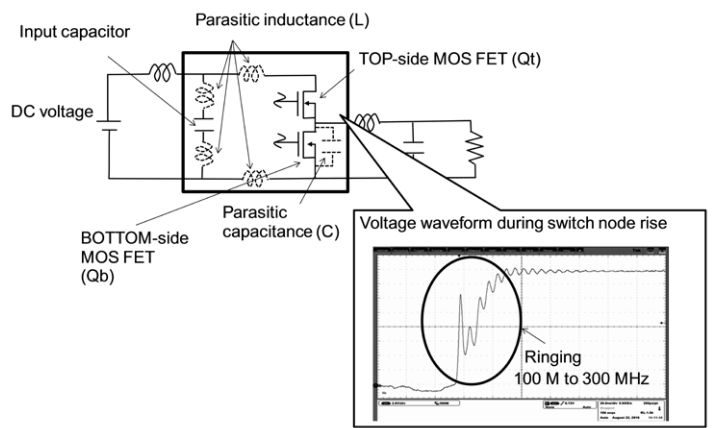


Fig. 3 DC/DC converter circuit ringing

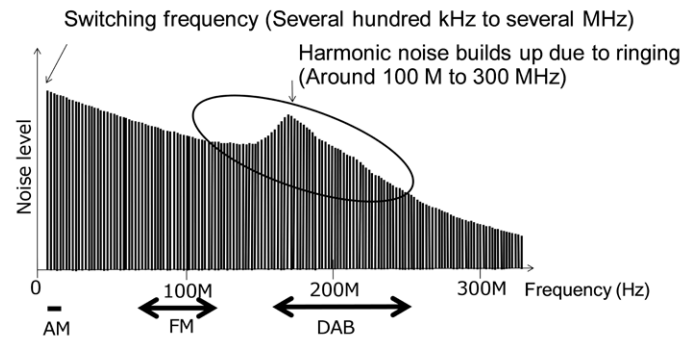


Fig. 4 Example of noise increase due to ringing

It is necessary to understand the effect of this harmonic and ringing noise in the initial stage of design and include EMC design in the product.

3. Trends in noise simulation analysis methods

3.1 General analysis method

The following shows a general analysis method linking circuit simulation and electromagnetic field simulation in order to include EMC design in the initial stage of design (Fig. 5).

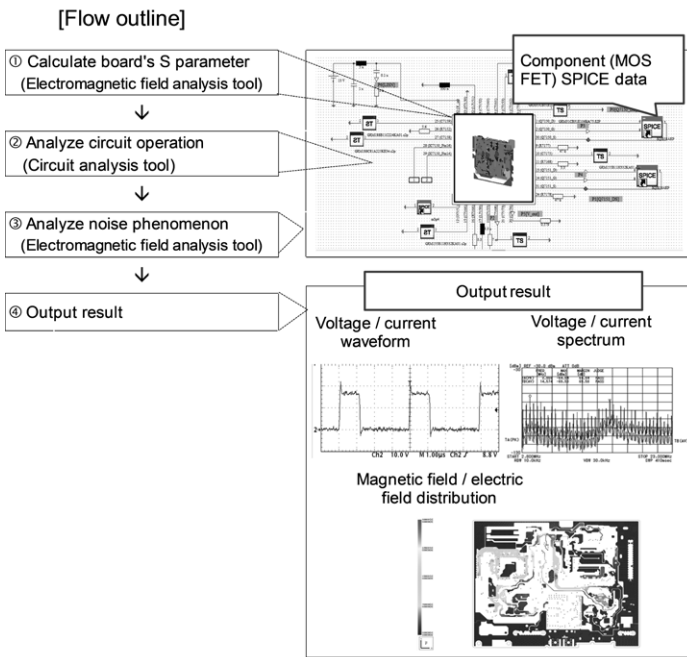


Fig. 5 Linked analysis of circuit analysis and electromagnetic wave analysis tools

- ① Calculate the board wiring S parameter using an electromagnetic field simulation analysis tool.
- ② Combine the output result from ① and the SPICE data of the component (MOS FET) and execute circuit operation analysis using the circuit simulation analysis tool.
- ③ Load the output result of ② into the electromagnetic field simulation analysis tool and execute analysis of the noise phenomenon.
- ④ Output results such as the voltage/current waveform and spectrum and the magnetic/electric fields distributions.

3.2 Problems of general analysis method

While the general analysis method can be used to confirm the circuit operation waveform and EMC properties, it often cannot be used in ECU development due to the following problems. Below, they are shown in order of importance (Q: quality, D: execution period, C: cost).

Problem 1 : Difficulty in executing correct analysis (Q: quality)

In circuit simulation analysis, it is difficult to acquire the SPICE data for the component (MOS FET) required in analysis. Also, even if it can be acquired, the data has poor accuracy and it is difficult to execute correct analysis.

Problem 2 : Difficulty in quick analysis (D: execution period)

In electromagnetic field simulation analysis, the high density and complexity of the board wiring and other factors necessitates a massive amount of time for calculation.

Problem 3 : Expensive operation cost (C: cost)

In addition to circuit simulation analysis, generally, expensive operation cost for electromagnetic simulation analysis is involved.

3.3 Setting development target values

To solve these matters, we devised and developed a new noise simulation method that allowed ECU development designers themselves to include the EMC design in the initial stage of design. For development, we set the following targets from the conditions necessary for use in the initial stage of ECU design (Table 1).

Analysis accuracy (Q) :

ECU individual difference and range of variation for actually measured values

Execution period (D) and cost (C) :

Period and cost required in ECU development

Table 1 Development target values (New method)

Target item			General method	Target value (New method)
1	Q	Difference from actual measurement	Max. 33%	Within 10%
		Frequency Level	Max. 9 dB	Within 6 dB
2	D	Calculation execution period	Around 2 weeks	Within 1 day
3	C	Operation cost	-	Compared to current -75% or more

4. Development of new noise simulation analysis method

4.1 Devised noise analysis method

To achieve the development targets mentioned above, we adopted a PI (Power Integrity) simulation analysis tool as our simulation analysis tool, which can easily perform modeling and high-speed analysis. As the tool is relatively inexpensive, we were able to lower operation cost. Here, we devised a noise analysis method that could be executed in a short period of time without impairing the analysis accuracy. The flow is shown in Fig. 6.

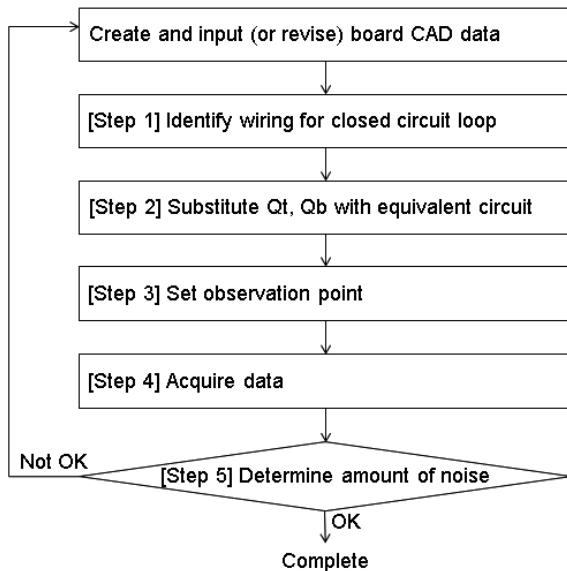


Fig. 6 Flow chart for the devised noise analysis method

The operation procedure is as follows.

[Step 1] To analyze in a short period of time, perform modeling for the wired part of the board with significant noise and perform calculations. Specifically, as Qb recovery current and the parasitic inductance L in the loop comprising the input capacitor Qt and Qb (bold frame in Fig. 7) cause energy of $1/2 \times L \times I_r^2$ to be accumulated and released, analyze this closed circuit.

[Step 2] The SPICE data of the component (MOS FET) is not used, because it is hard to be acquired and has poor accuracy. Limit analysis to the operation of the moment noise occurs, and substitute the component with an equivalent

circuit without analyzing the switching operation. Specifically, as the recovery current I_r of the BOTTOM-side MOSFET (Qb in Fig. 7) is the origin point of the noise, substitute this with an electrical current source. At this time, as the TOP-side MOSFET (Qt in Fig. 7) is ON, substitute this with a short-circuited equivalent circuit.

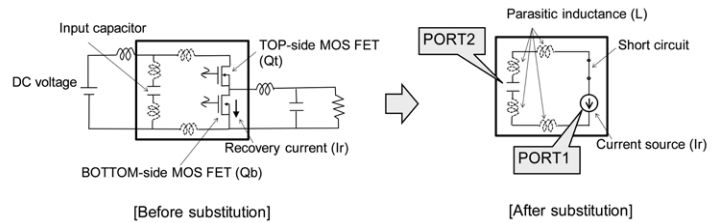


Fig. 7 Equivalent circuit substitution for the closed circuit loop

[Steps 3, 4] Use the Z parameter broadly used in PI simulation analysis to evaluate the impedance characteristics. Regarding radiation noise, to evaluate the degree of inhibition for noise radiation from the board, set the electrical current source to the observation point "PORT1" and acquire data for input impedance "Z11" looking at the board. On the other hand, regarding conduction noise, to evaluate the conduction noise of the board connector terminal, set the input capacitor close to the connector terminal to the observation point "PORT2", acquire the conduction impedance "Z21" from the electrical current source "PORT1" to "PORT2". To identify locations with poor board wiring in frequencies where Z parameters (Z11, Z21) are large, acquire the "near-field noise distribution" (Fig. 8).

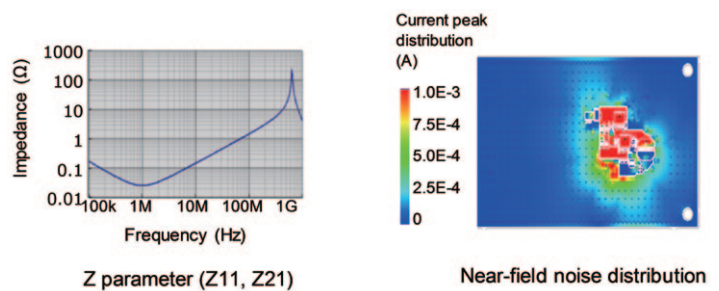


Fig. 8 Example acquired data

[Step 5] Repeat the steps 1 to 4 in the same way for several boards with changes to the board wiring and other specifications. Compare the data acquired from these analyses to select a board with a minimal amount of noise.

In this way, efficient EMC design can be included from the initial stage of design.

The following shows comparison of this new analysis method and the general analysis method (Table 2).

Table 2 Comparison of noise analysis methods

Noise analysis method	New method	General method
	PI analysis	Circuit and electromagnetic field analysis
Switching operation (ON/OFF)	Not present (Only moment of noise occurrence)	Present
Power source/ GND wiring	Partial (Only closed circuit with significant noise)	All
SPICE data	Not necessary	Necessary
Advantages (What can be done)	Few work hours, short period of time (1 day)	Can confirm circuit operation waveform and EMC characteristics
Disadvantages (What cannot be done)	Cannot confirm circuit operation waveform	Requires work hours and time (2 to 3 weeks), difficult to get accuracy

4.2 Verification

4.2.1 Verification method

In order to confirm whether the new analysis method meets the necessary criteria, we proceeded with verification using a verification board. Furthermore, in order to confirm that a board with a minimal amount of noise can be selected assuming actual operation, we created two types of boards with different areas for the closed loop (bold frame in Fig. 7), which has a significant impact on noise, and compared the results (Table 3).

Table 3 Board artwork specifications

	Layer 1	Layer 2	Layer 3	Layer 4
Small loop (Standard)				
Area: 117.45 mm ²				
Large loop (Area x4)				
Area: 469.80 mm ²				

4-Layer board 1.6 mm thickness, board exterior size: 110 mm x 60 mm

The acquired data was handled as the radiation and conduction noise for the AM, FM, and DAB bands (Fig. 9). Verification was implemented in two steps. These are shown below.

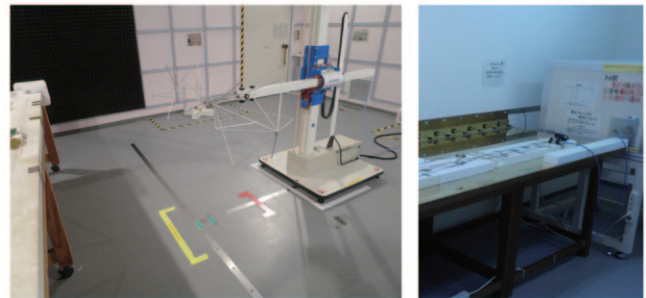


Fig. 9 Measurement status in anechoic chamber (Left: Radiation, Right: Conduction)

Verification (1) : Optimizing the simulation method

We applied quality engineering to determine setting conditions with high accuracy for the PI simulation analysis tool.

The basic function outputs a simulation result close to the actual measured result of an actual device. The characteristic value is evaluated as the peak value for the noise voltage in the simulation result using the zero-point proportional expression (Fig. 10).

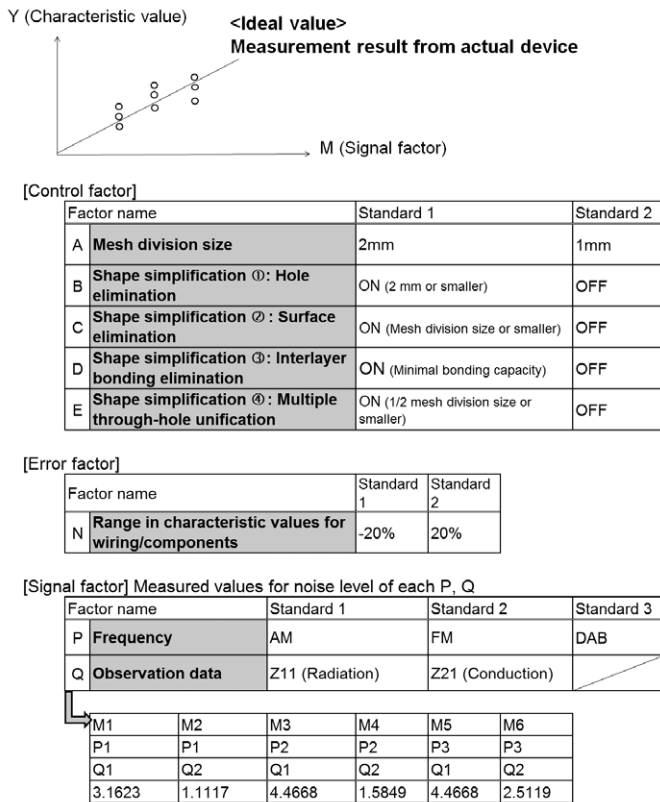


Fig. 10 Determining each factor and standard in quality engineering

Verification (2) : Correlation between the simulation and actual measurement

The correlation between the measured data and the simulation data is confirmed.

4.2.2 Verification result and observations

Verification (1) : Optimizing the simulation method

The setting that divided the board pattern into mesh form for simulation analysis (factor A) had a significant contribution ratio to the signal-to-noise ratio and sensitivity and significantly affects analysis accuracy. On the other hand, the results showed that settings that simplified the minute shapes of the board pattern (factors B to E) had a small impact on the analysis accuracy.

As the optimization conditions required a significant signal-to-noise ratio and sensitivity as close to zero as possible, we selected factor A1. For factors B to E, as their impact on the analysis accuracy was small, we adopted settings that enabled calculations within a short period of time (factors B1, C1, D1, and

E1). We held confirmation experiments to confirm the reproducibility of the gain. As the result, with respect to the estimate of $100 \pm 30\%$, the sensitivity was almost within the scope (66.0 to 100.7%). On the other hand, while the signal-to-noise ratio was larger than the estimate (a maximum of 196.4%), it was the result compared to less than 1 db, and there was no problem (Fig. 11).

In this way, as we confirmed the reproducibility of the gain, we were able to optimize the simulation method (Table 4).

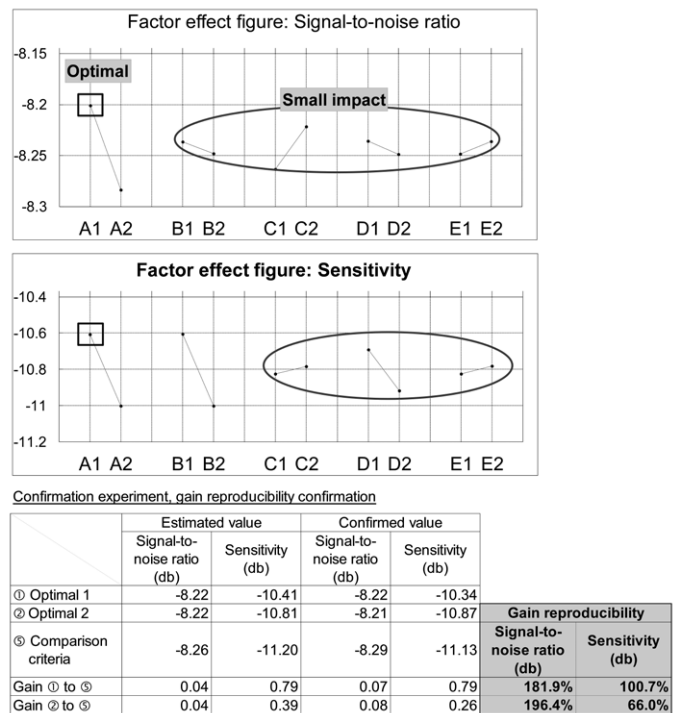


Fig. 11 Investigation result for simulation method

Table 4 Simulation optimization setting criteria

Setting item	Optimal setting	Note
A Mesh division size	2 mm	Requires adjustment based on board specifications
B Shape simplification ①: Hole elimination	ON (2 mm or smaller)	-
C Shape simplification ②: Surface elimination	ON (Mesh division size or smaller)	-
D Shape simplification ③: Interlayer bonding elimination	ON (Minimal bonding capacity)	-
E Shape simplification ④: Multiple through-hole unification	ON (1/2 mesh division size or smaller)	-

Verification (2) : Correlation between the simulation and actual measurement

We confirmed the correlation between the simulation data and the measured data. As for the AM and FM bands, they are within target values for both the frequency and level. Correlation to the level could

not be acquired in some frequencies for the DAB band (170 M to 190 MHz) (Fig. 12, Table 5).

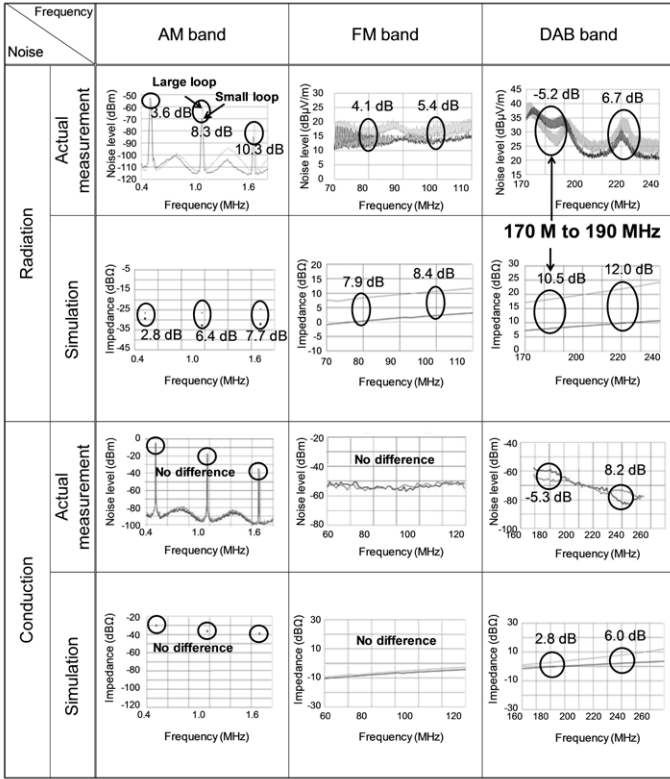


Fig. 12 Comparison of actual measurement and simulation

Table 5 List of correlations between actual measurement and simulation

		AM band 0.51 M to 1.71 MHz	FM band 76 M to 108 MHz	DAB band 174 M to 240 MHz	
Target value	Frequency	Within 10%			
	Level	Within 6 dB			
Result ^{*1}	Radiation	Frequency	[Yes] 2.5%	[Yes] 3.2%	[Yes] 2.0%
		Level	[Yes] 2.6 dB	[Yes] 3.8 dB	[No] 15.7 dB
	Conduction	Frequency	[Yes] 2.0%	[Yes] 2.0%	[Yes] 1.0%
		Level	[Yes] 0.4 dB	[Yes] 2.0 dB	[No] 8.1 dB

*1 Legend
 Yes: Correlation present (Target value met)
 No: No correlation

5. Evaluation of this analysis method

We evaluated the development target values set in Section 3.3 from a QCD point of view. The result is as follows (Table 6).

Table 6 Evaluation result for the new noise analysis method

		Target value	Result	Achieved	
Q	Frequency	AM	Difference from actual measurement	2.5%	Yes
		FM	Within 10%	3.2%	Yes
		DAB	Within 10%	2.0%	Yes
	Level	AM	Difference from actual measurement	2.6dB	Yes
		FM	Within 6 dB	3.8dB	Yes
		DAB	Within 6 dB	15.1dB	No
D	Calculation execution period	Within 1 day	4H to 12H	Yes	
C	Operation cost	-75% compared to current	-89% compared to current	Yes	

Q : Excluding the DAB band levels, we achieved all other targets.

D : Calculation time was approximately 10 minutes for the four-layer board used this time. When considering the circuit scale, the numbers of boards and their layers, and other factors, we can estimate a time of 4 to 12 hours for our actual products.

C : Because we were able to operate using only a PI simulation analysis without the need for a generally expensive electromagnetic field simulation analysis, we were able to significantly reduce cost, by 89% of the current cost.

From the above results, excluding the DAB band levels for Q, we achieved all other targets. Therefore, this can be utilized to develop an ECU in a short period of time with low cost in the AM and FM band frequencies. Regarding the level for frequencies in the DAB band and above, we will confirm the overall frequency characteristics including outside the frequency range in future investigations to determine the cause.

6. Conclusion

Here, we were able to adopt a PI simulation analysis tool, which could easily be used even by a person who is not an EMC expert, to devise and develop a noise analysis method for DC/DC converters. We believe that this will enable ECU development designers to efficiently and effectively include EMC design from the initial stage of design themselves.

We will use this new analysis method to

accumulate data to find trends for accuracy in high frequencies as well as optimization measures to use broadly in ECU development. Also, at the current point in time, we have applied our investigations to the step-down circuit of a DC/DC converter on a board; however, in future, we will expand the scope of application to include step-up/down circuits, unified analysis for a board and chassis, and other areas.

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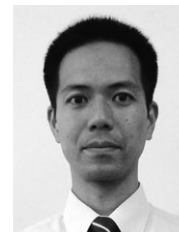
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