All-CMOS Process Engine Control System LSI Chip

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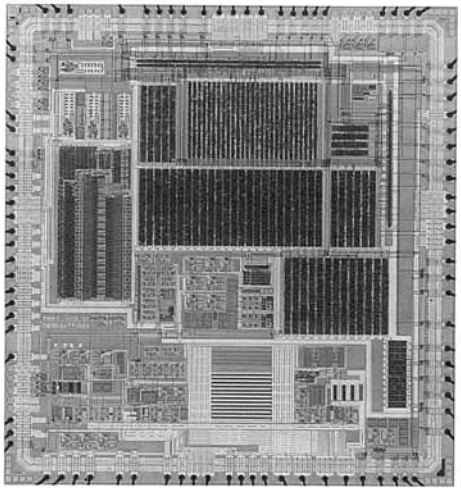

We have developed more than forty(40) custom ICs (ASICs) to meet continuously increasing needs of high performance, small sized, light weighted, and lower price engine control units (ECUs) for automobile applications.

Although most of those ASICs are of single function, we have newly developed an all-CMOS process ASIC with Fujitsu Limited on which multiple functions, i.e. power supply, knocking control circuitry, engine revolution sensor processors, level interface circuitry , and so on, are integrated. The ASIC will be onto a market in April 1997 on engine management ECUs.

This paper describes the functions and characteristics of the ASIC and some design tips are also introduced.

1. Introduction

While improving in functionality and performance, automotive electronic equipment are also expected to be compact, lightweight, and economical. To meet these demands, Fujitsu TEN has been offering individual functions in custom ICs.

Fujitsu used to meet the needs of electronic equipment for engine control with custom ICs, but can no longer compete with other manufacturers in terms of price by using the conventional IC development method. To make ICs even smaller and more economical, we developed a system LSI chip jointly with Fujitsu Limited by integrating several IC functions on a single chip.

This paper describes the functions and characteristics of the system LSI chip, and the design techniques.

2. Outline of system LSI chip

The system incorporated almost all the functions that used to be mounted on an engine control unit (ECU), as shown in Figure 1. This chapter explains how to realize digital and analog circuits as a system LSI chip.

2.1 Objectives of the system LSI chip

When developing the system IC, we determined the basic concept with priority given to "potential" and "costs."

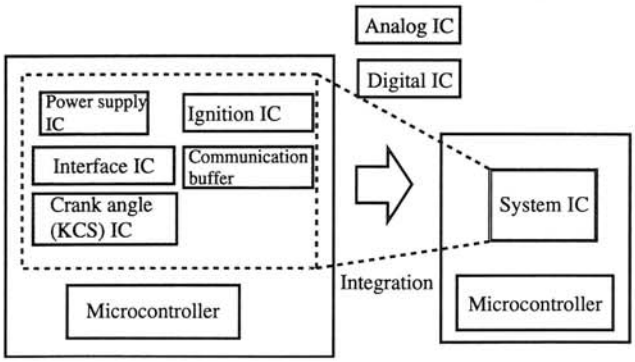

Figure 1. Outline of engine control system LSI

2.1.1 Process selection

Although other manufacturers are also developing system ICs for engine control, they mainly use the Bi-CMOS process.

By comparing the IC processes from the viewpoint of potential and costs, as in Table 1, we determined the CMOS process to be the most promising for our system LSI chip. The CMOS process is advantageous for high integration because the technology used for fine patterning is improving fast and the cost performance is increasing every year. There is no doubt that the CMOS process will be come the major IC process.

Table 1 Circuit conformance and features of processes

		Process		
		Bipolar	CMOS	Bi-CMOS
Conformance	Analog IC	◎	△	○
	Digital IC	×	◎	○
	Analog-digital hybrid IC	×	○ (Fujitsu)	◎ (Other vendor)
Feature	Cost	◎	○	×
	Potential	△	○	△

It is essential to integrate a microcontroller , a critical system component, and its peripheral functions in order to survive in the anticipated severe price competition. We considered the CMOS process to be optimal for realizing this integration.

The only problem was in implementing a high-precision analog circuit. We solved this problem by developing new cells and changing the conventional analog circuits to digital. This solution is detailed later.

2.1.2 Features of the CMOS process

Fujitsu's Quickly Customized Microcontroller (QCM) technology was used for developing the system LSI chip. This technology based on the 0.8 μm process offers various analog and digital macros, such as high-speed AD converters, comparators, and operational amplifiers.

2.2 Outline of function blocks

This section mainly outlines the individual function blocks.

2.2.1 Power supply block

The power supply block reduces the battery voltage and keeps the rated supply voltage for each part. The engine control ECU requires two power supplies. This block has the following functions:

① Main power supply (VCC) and backup power supply

The VCC supplies power (5 V) to the microcontroller and the IC and its peripherals. At ignition, power to the microcontroller is supplied from the backup circuit. Figure 2 shows the operations of the backup circuit. When the ignition is turned on, the VCC voltage increases. Once the VCC voltage has exceeded the VDD voltage (see ②), the backup transistor connected to the VCC and VDD is turned on and the VDD voltage rises closely along with the VCC voltage. The backup transistor used to be an external part, but was built into the system IC after cost studies.

To avoid adjustment of the battery voltage detection resistance as a function of the engine control ECU, the VCC accuracy was designed with the precision of ±1% (at room temperature), including battery and VCC load fluctuations. See 3.2.2 for the reason and design technique.

② Standby power supply (VDD)

The microcontroller in the engine control ECU has a read-write memory device of low current consumption called standby RAM to store vehicle aging information and learned control parameter information. The VDD supplies power (3.3 V) to the standby RAM to keep the information even when the ignition is turned off. This circuit was designed with the precision of ±5% because a high-preci-

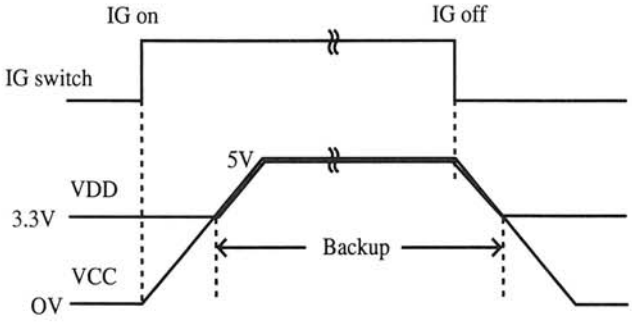

Figure 2. VDD Backup

sion supply voltage is not required for keeping the contents of the standby RAM.

③ Reference power supply (VREF)

Since the VREF is used as the reference power supply for the VCC, VDD, and other circuits, its precision directly affects the precision of the power supply. The VREF precision is the most important factor for enhancing the VCC precision. See 3.2.2 for details.

④ 8 V detector

The 8 V detection circuit monitors the battery voltage (+B) when the ignition is turned on. This circuit notifies the microcontroller of a low battery voltage (8 V or less) at cranking (battery voltage drop when the engine is started at a low temperature) or when the ignition is turned off. If this signal is received, the microcontroller inhibits the writing of diagnostic results in the standby RAM to prevent a diagnostic error.

⑤ VCC voltage detector

The microcontroller may malfunction if the VCC voltage falls below the rated minimum supply voltage of the microcontroller when the ignition is turned off or at cranking. This malfunction is prevented by three types of reset functions: power-on reset, low-voltage reset, and runaway reset. (For details, refer to Fujitsu TEN Technical Report Vol. 5, No. 1, 1987.)

The reset block used analog circuits until row. This LSI chip, however, uses an analog circuit for detecting a low VCC voltage and a digital circuit for setting the microcontroller reset time. See 2.2.6 for the reset functions.

2.2.2 Crank angle signal processing block

The crank angle signal processing block detects a zero crossing by comparing the engine revolution (NE) and cylinder discrimination (G) signals, and shapes the waveform. This block consists of an analog unit, a digital unit, and a 6-bit DA converter. The analog unit shapes the waveform of a crank angle sensor signal with a comparator. The digital unit generates a mask signal to eliminate noise when shaping the waveform. The 6-bit DA converter outputs the G-signal threshold level.

Since the crank angle signal suffers from noise at ignition, the conventional IC eliminates this noise at waveform-shaping by using a capacitor. The system IC, however, uses an output masking digital circuit to eliminate noise. Figure 3 shows the noise elimination methods of the conventional IC and the system IC.

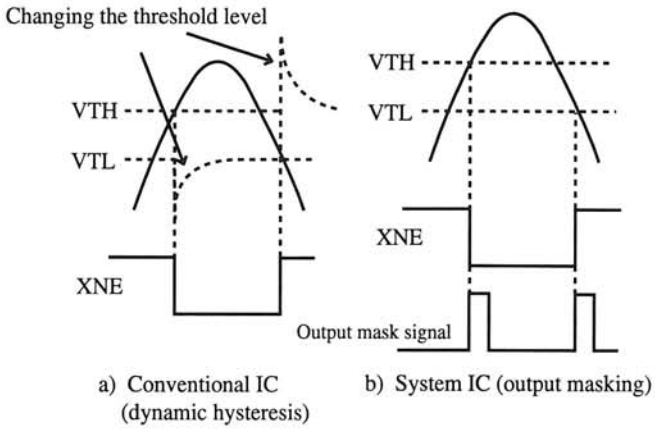

Figure 3. Noise elimination methods

The masking time of the output mask signal is varied with the number of engine revolutions by counting the number of NE signals entered within a specified time, as shown in Figure 4. To make the G-signal threshold level dependent on the number of engine revolutions, we applied F/V conversion to the NE signal frequency using a digital circuit counter and a 6-bit DA converter. Figure 5 shows the threshold level characteristics we achieved.

2.2.3 Knock sensor signal processing block

The knock sensor signal processing block consists of a peak detector and a fail processor. The peak hold signal holds the peak of a knock sensor signal (hereafter, knock signal) output when the engine knocks. The fail processor detects sensor and sensor signal line errors.

The conventional IC uses a bipolar process which offers high precision in analog circuits. However, it is difficult to achieve the necessary precision with the CMOS process used for the system IC. To achieve this level of precision, we created the block from a high-speed AD converter, a digital processing circuit, and an amplifier to ensure the gain. Figure 6 is a block diagram of the knock sensor signal processing block.

The conventional IC used to charge its capacitor with the knock signal voltage to hold the peak. Because of the time constant, the IC could not follow quick changes in the knock signal.

By using a high-speed AD converter, the system IC samples knock signals of about 5 to 10 kHz at 500 kHz. The maximum value of the sampled signals is serially transferred to the microcontroller as the peak hold value through digital processing. This method enhances the peak hold characteristic, as shown in Figure 7. High-speed sampling

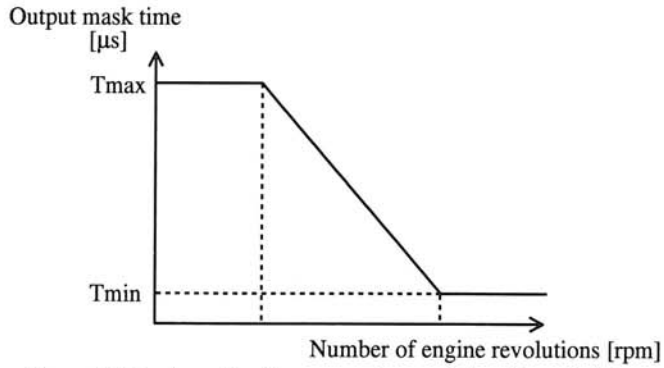

Figure 4. Output masking time vs. engine revolution characteristic

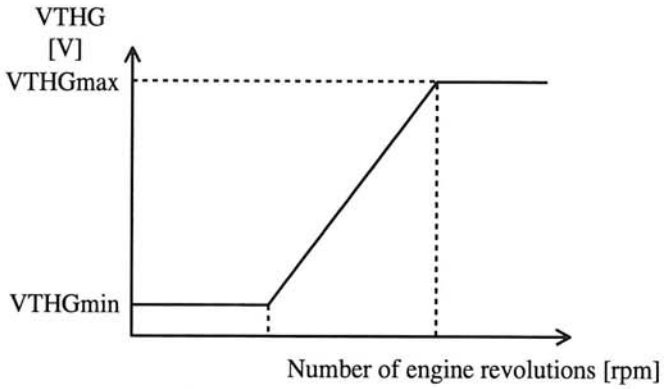

Figure 5. GTGH vs. engine revolution characteristic

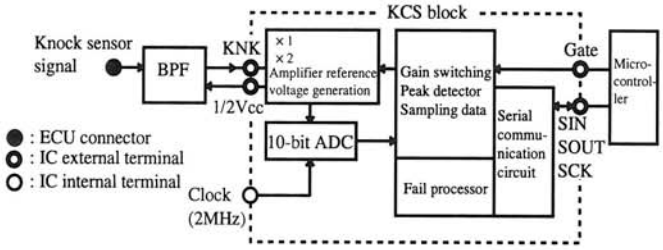

Figure 6. Block diagram of knocking sensor signal processing

is also applicable to future knock detection signals of high frequencies.

The input knock sensor signal of the conventional analog IC is the reference voltage 0 V ± 5 V. Since the peak value is the minimum value of the waveform below the reference voltage, the IC has a 5 V dynamic range. The input voltage range of this system IC, however, is limited because the CMOS IC cannot tolerate high voltages. Therefore, the knock signal should be attenuated to the reference voltage 2.5 V ± 2.5 V. (Figure 8)

Despite the disadvantage of having half the dynamic range, we adopted the gain switching method because an especially high voltage is required for control only at a

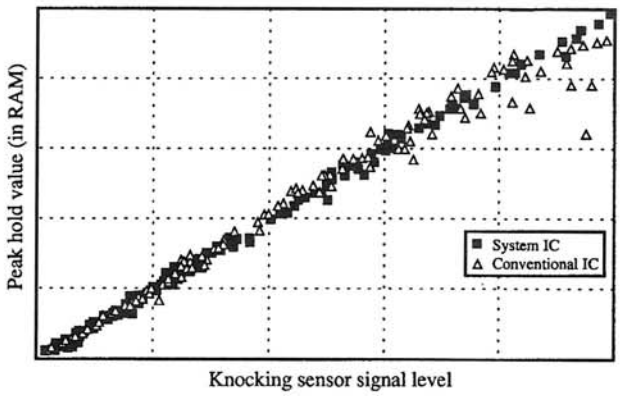

Figure 7. Peakhold characteristic

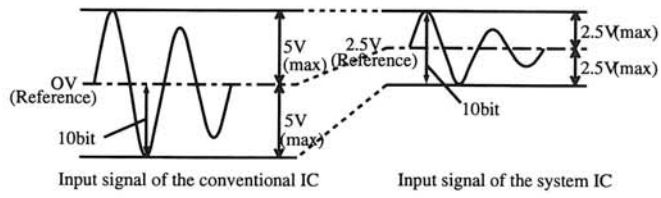

Figure 8. Comparison of dynamic range

narrow amplitude. If the input signal has a small amplitude, it is doubled to achieve the same resolution as before. Figure 9 shows an outline of this function.

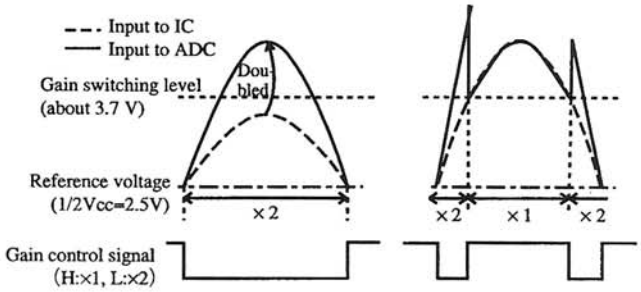

Figure 9. Gain control of knocking sensor signal

2.2.4 Interface block

The interface block converts digital input signals from the sensors (vehicle speed and starter signals) to satisfy the microcontroller port input specifications. This block has the following IC functions:

① Interface circuit (three built-in channels)

The interface circuit outputs signals received from various sensors without inversion and supports comparator input. This circuit can receive sensor signals through three channels.

② Starter signal processor

The starter signal processor outputs starter signals without inversion and supports comparator input. However, since the starter signal input level varies with the battery voltage, the comparator threshold level is made dependent on the battery voltage.

③ Communication buffer

The communication buffer uses serial communication between the computer and ECU micrcontroller for carrying out a diagnosis.

2.2.5 Ignition control block

For ignition control, either the ESA-A/B or ESA-CII crank angle system can be selected by setting the external terminals. This block mainly has the following functions:

① Ignition mode switching control
② Ignition signal distributting control (ESA-CII only)
③ Crank angle position detection (ESA-CII only)
④ Signal masking during starter on
⑤ Fuel pump control

Ignition mode switching control sets the hard (fixed) ignition mode when microcontroller reset is detected and the soft (CPU) ignition mode when normal microcontroller operation is detected.

2.2.6 Reset control block

The reset control block controls the low-voltage detection signal output from the power supply block, the INIT signal to reset the microcontroller by the timer, and the HALT signal to stop the microcontroller clock oscillation.

The microcontroller is reset in two cases:

One is when a low voltage is detected. The reset block resets the microcontroller immediately if a low voltage is detected.

The other is when the watchdog timer (WDC) is abnormal. The reset block always monitors the WDC signal output from the microcontroller and resets the microcontroller if the WDC signal is found to be abnormal.

Once the WDC signal has become normal or the supply voltage recovers after a low-voltage reset, the INIT or HALT signal is released a specified time later (restart function). As described in 2.2.1, the restart function is built in the conventional power supply IC as an analog circuit but a digital circuit in the system IC.

A timer function is required for the above operation. The conventional IC requires an external part for the timer function using the capacity charge and discharge time. However, the system IC does not because the timer function operates on the built-in clock. Figure 10 is an operational chart of this function.

2.3 IC test method (Test circuit)

The system IC integrates six digital circuits as function blocks. Their input and output terminals are mutually connected in the IC and their signal wires may not lead to external terminals of the IC. If signals from each function block do not lead to external terminals, all the related blocks must be operated to test one block.

Therefore, a great many test patterns are required but not all the functions may be tested. If the internal signals are led out for the test, the number of terminals increases, and this affects the package size. To test each function block securely without increasing the number of terminals, we built in a test circuit.

3. System IC design techniques

This chapter explains the techniques used to develop the system IC.

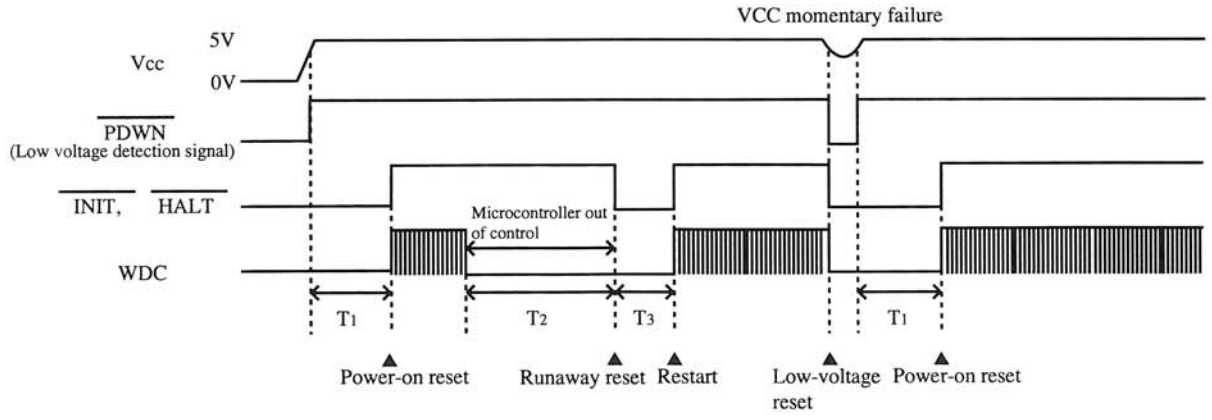

Figure 10. Reset control sequence

3.1 Developing new cells

The current QCM library cells are not adequate for realizing a high-precision analog circuit, so we designed the following cells:

① Low-offset operational amplifier

The offset voltage of the existing operational amplifier is ±10 mV. By ensuring device-matching (cross-matching) when designing the layout, we developed a new operational amplifier whose offset is ±7 mV.

② Zero-cross comparator and rail-to-rail operational amplifier

The input voltage range of the existing operational amplifier and comparator is from the GND voltage + 1.25 V to the supply voltage VCC - 1.25 V. (When the supply voltage is 5 V, the input voltage range is from 1.25 to 3.75 V.) Therefore, we designed a zero-cross comparator that operates at the input voltage from 0 to 3.75 V (supply voltage = 5 V) and a rail-to-rail operational amplifier that operates at the input voltage from 0 to 5 V (supply voltage = 5 V).

3.2 Designing the power supply block

3.2.1 Configuration by the process of low threshold voltage

The conventional power supply block allows the direct connection of a battery voltage (usually 6 to 18 V) to the IC because a 35 V bipolar process is used.

However, since the process of the system IC withstands only 7 V, the battery voltage cannot be applied to the IC terminal directly. To solve this problem, we developed a new power supply block. Figure 11 compares a conventional power supply block and the new one.

For the VCC circuit and internal power supply (VR) circuit, a PNP transistor and an NPN transistor are prepared as external parts and a high voltage is applied to the emitter and base (collector) of the NPN transistor. The VR circuit supplies power (5 V) only to the power supply block of the system IC for the VREF and VCC overcurrent limiting circuit.

The conventional overcurrent limiting circuit consists of a current detection resistor connected to the emitter side of the PNP transistor for VCC control (boost transistor). In this configuration, a battery voltage is applied to the terminal where the above resistor is connected. Therefore, the current detection resistor is connected to the collector side of the boost transistor in the system IC to reduce the voltage applied to the IC terminal.

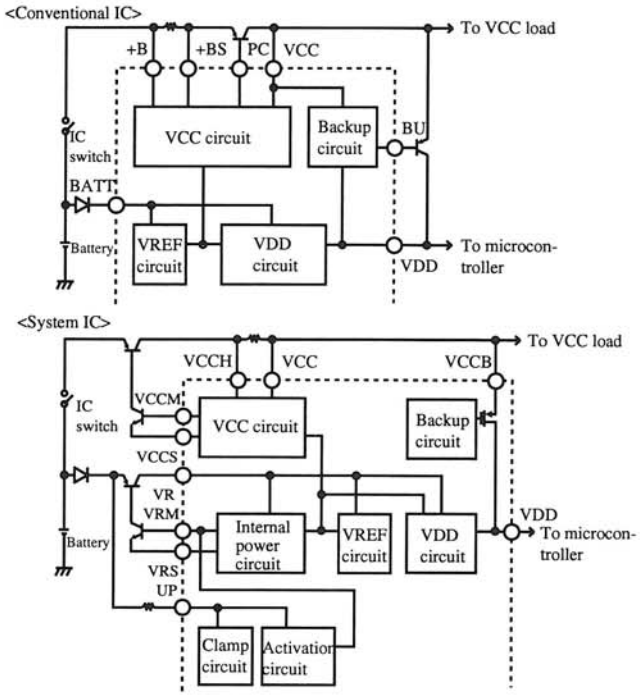

Figure 11. Schematics of voltage regulator

3.2.2 Enhancing the VCC voltage precision

Figure 12 shows the VCC regulator for VCC voltage control. This regulator controls the VCC voltage to satisfy the following equation:

$$Vref+Vof= R2/(R1+R2) \times Vcc$$

Vref: Reference voltage (generally, 1.24 V)

Vof: Offset voltage of the operational amplifier

R1,R2: VCC voltage dividing resistor

VCC in the above equation can be changed to the following:

$$Vcc= (Vref+Vof) \times (R1+R1) /R2$$

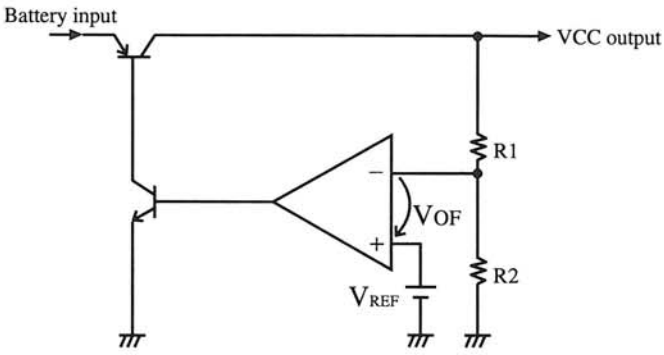

Figure 12. VCC voltage regulator

Therefore, the VCC voltage precision (ε) is the sum of three types of precision shown below:

$\varepsilon = \varepsilon 1 + \varepsilon 2 + \varepsilon 3$

$\varepsilon 1$: VREF voltage precision

$\varepsilon 2$: Vof voltage precision

$\varepsilon 3$: Specific precision of R1 and R2

Since $\varepsilon 1$ is generally about ±4%, the trimming method is used to reduce the VCC voltage to ±3% or less. Trimming is a method of adjusting the VREF to set the VCC voltage within the standard range.

For the system IC, the precision of 0.5% obtained by trimming to achieve the VCC precision of ±1% (at the room temperature) prescribed in 2.2.1.

The number of bits necessary for trimming is:

$1.441n\ (a/b)$

a: Process dispersion (same as ε above here)

b: Desired precision

For the system IC, $a = \varepsilon = \pm 10\%$, $\varepsilon 1 = \pm 8\%$, $\varepsilon 2 = \pm 1\%$, $\varepsilon 3 = \pm 1\%$), and $b = \pm 0.5\%$. If these values are assigned to the above, the number of bits necessary for this IC becomes about 5 bits (4.314).

According to this equation, we could realize a VCC voltage precision of ±1% (at room temperature, including the battery voltage and load fluctuations).

3.2.3 Reducing the dark current

The dark current is the current consumed by the IC when the engine (ignition) is switched off. The purpose of reducing this current is to prevent a dead battery. To reduce the dark current, we attempted to reduce the current consumption by unused circuits to zero when the ignition switch is off. This attempt reduced the dark current to 50%.

3.3 Digital circuit verification using FPGA

The conventional circuit design method for digital ICs is by CAE simulation only. For the system IC, we replaced many analog circuits with digital ones. Digital circuits require not only simulation but verification by actual system operation (engine on) to see that the control is valid for digital processing. For this verification, we adopted a breadboard (BB) using a field programmable gate array (FPGA).

The FPGA is a programmable gate array. With this, designed logic can be realized immediately by the user because no masking is required.

We evaluated the knock signal processing and crank angle signal processing circuits on a vehicle by this method and proved that the circuits can be controlled by digital processing.

Circuit verification using the FPGA can find an error at the design stage. On-vehicle evaluation is useful for verifying an operation under unusual input conditions that cannot be simulated. Therefore, we could correct circuit defects before mask release.

Since the design environment was not prepared for the current IC development project, we had to enter the circuit diagrams and test patterns in another CAD system. By adopting design techniques based on the Verilog HDL and other hardware description languages (HDLs), we will establish a unified design environment, as shown in Figure 13.

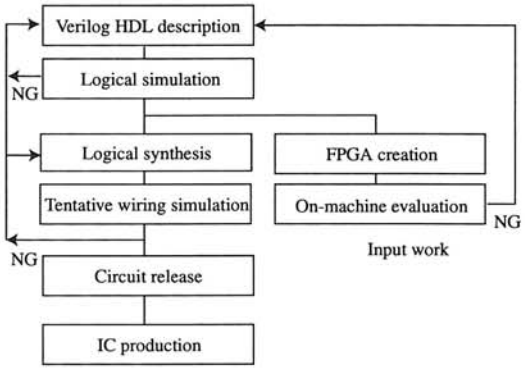

Figure 13. HDL design

4. Future development

4.1 Integration the microcontroller

Integrating the microcontroller will be the first step in the future development of the system IC. As mentioned before, we selected the CMOS process for this IC by considering this.

These days, we often hear the phrase "system on silicon." This implies the integration of many on-board ICs into a single chip. In the age of fierce competition, we are also seeking for an LSI chip of this type.

Microcontroller technology is upgraded every year and now the 0.35 μm process is becoming popular. A microcontroller cannot be integrated on the system IC by the 0.8 μm process because of the restricted chip size. Therefore, we should discuss development using a more advanced technology. Matching of the analog circuits will be the largest obstacle.

High-speed microcontroller operations by fine processing technology may increase radiation noise. We must design an IC carefully to minimize such noise. For automotive use, the noise insulation is also an important factor. The 0.35 μm process makes a digital unit susceptible to the influences of external noise because the unit operates on 3 V. To solve this problem, we should establish a noise simulation technology and incorporate noise reduction measures at the design stage.

4.2 Changing analog circuits into digital ones

As mentioned in Chapter 2, the CMOS process is suitable for digital circuits but does not satisfy the requirements of precision and chip area for analog circuits. Therefore, we changed analog circuits into digital ones for the system IC.

To integrate a microcontroller in future, the peripheral circuits must also be made digital.

The following advantages are obtained by making the circuits digital:

① A microcontroller can be interfaced easily.
② An IC can be developed using the latest technologies.
③ Verification by simulation is comparatively easy.

This also gives rise to the following disadvantages:

① Radiation noise increases.
② The circuit scale may have to be extended.

We will keep developing LSI chip suitable for automotive use while tackling the above problems by perfecting the technologies of simulation and hardware description design. These efforts will reduce the development cycle, enhance the design quality, accumulate design assets, and make the assets effectively available.

4.3 Designing analog-digital hybrid circuits

As mentioned so far, the system IC has a hybrid configuration consisting of digital and analog circuits. We designed the circuits separately and verified them using a circuit simulator. However, we could not verify a hybrid circuit like the A/D converter by desktop calculations because the introduction an analog - digital hybrid IC simulator into the design environment had not been discussed yet.

Fujitsu TEN is now discussing the introduction of a design tool available for simulating an analog - digital hybrid IC circuit and the construction of a simulation environment using a high-level language. Table 2 lists the design tools now under discussion.

Table 2 Design tools under discussion

	Present tool	New tool under discussion
Analog	Spice circuit simulator (Hspice)	Verilog-A SpectreHDL HspiceHDLA VHDL-A(Saber)
Digital	Fujitsu logical circuit simulator (ViewCAD)	HDL (Verilog HDL already introduced)

5. Conclusion

Production of the system IC will begin in 1997. Adopting this IC will greatly reduce costs of the engine control ECU.

We think the successful development of the system IC has almost established the analog circuit design technology using the CMOS process. The possibility of a digital control system was also verified. By using these design techniques and assets, we can promote the future development of large-scale hybrid ICs.

People will strongly expect automotive electronic equipment to be more compact and lightweight, and to cost less. The growing demand for automotive multimedia equipment will make competition even fiercer.

Fujitsu TEN will apply the design techniques learned in the development of this system LSI chip to the fields of not only automotive electronic equipment but also car audio and multimedia equipment. The design techniques will help us develop LSI chips conforming to the requirements of the day and satisfy the customer needs.

Finally, we thank FUJITSU VLSI LIMITED and other parties for their cooperation in this project.

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