Reception performance improvement of AM/FM tuner by digital signal processing technology

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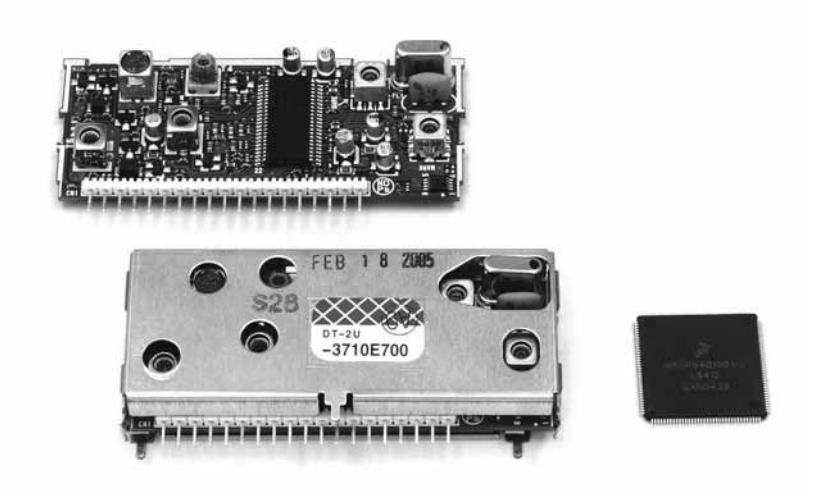


Abstract

With developments in digital technology, CDs, MDs, DVDs, HDDs and digital media have become the mainstream of car AV products. In terms of broadcasting media, various types of digital broadcasting have begun in countries all over the world. Thus, there is a demand for smaller and thinner products, in order to enhance radio performance and to achieve consolidation with the above-mentioned digital media in limited space.

Due to these circumstances, we are attaining such performance enhancement through digital signal processing for AM/FM IF and beyond, and both tuner miniaturization and lighter products have been realized.

The digital signal processing tuner which we will introduce was developed with Freescale Semiconductor, Inc. for the 2005 line model. In this paper, we explain regarding the function outline, characteristics, and main technology involved.

1 Introduction

In recent years, CDs, MDs, DVDs, and digital media have become the mainstream in the car AV market.

In terms of broadcast media, with terrestrial digital TV and audio broadcasting, and satellite broadcasting having begun in Japan, while overseas DAB (digital audio broadcasting) is used mainly in Europe and SDARS (satellite digital audio radio service) and IBOC (in band on channel) are used in the United States, digital broadcasting is expected to increase in the future. In addition, a state of technological maturity has been reached in AM/FM broadcasting, making it difficult to make further cost reductions and improvements in reception for conventional analog technology.

Through digital signal processing for AM/FM IF and beyond, we are attaining performance not possible with conventional analog signal processing, while also developing a car digital signal processing tuner that shares processing with future digital media.

In December 2004, this tuner was added to our lineup of products for 2005.

2 Development goals

2.1 Background

Although certain manufacturers have been developing products for the digital processing of AM/FM radio for approximately 10 years, little progress has been made over conventional products (those with analog processing of signals) in terms of performance and cost reduction. However, with the recent improvements in DSP performance, there have been significant reductions in cost.

The results of car ratings performed by JD Power, a North American consumer satisfaction indicator, showed that the cars with the highest ratings had radios with functions to prevent noise and interference from adjacent FM signals.

As mentioned above, it has become difficult to make improvements and differentiate with analog technology. With digital signal processing, performance can be improved for clear differentiation with other companies, but this had not yet been achieved due to the processing capabilities and cost-related issues of DSP.

Due to recent improvements in both signal processing performance and cost reduction in DSP, the standardization of radio signal digital processing DSP with other functions (specifically, the standardization of audio processing such as sound field controls with DSP) has resulted in the achievement of costs equal to and lower than conventional systems (analog processing tuners + audio processing DSP). In addition, through digital processing from IF signals, interference and noise prevention performance have surpassed those of analog systems.

2.2 Goals of digitalization

The following items were the goals in the development of this digital processing platform for radio:

①Improvements in performance (differentiation with other companies through software algorithms)

- Reduction in noise (improvements in AM/FM noise reduction performance, and FM multi-pass performance)
- Improvements in interference prevention (improvements in interference from adjacent AM/FM signals)

②Reductions in cost through functional integration (development of integrated radio processing/audio processing DSP)

③Miniaturization (reduction of large parts such as ceramic filters)

3 Outline of entire system

3.1 Outline of entire system

A system block diagram of the digital signal processing tuner is shown below.

It is made up of 3 primary parts.

①Tuner module

This module converts RF signals to IF signals, and outputs the IF signals. It is constructed of a tuner LSI and its circuitry, as well as a Memory IC that stores parameters. IF signals are then input to the analog interface.

②Analog interface

This interface converts the IF analog signals input from the tuner into digital signals. After the digital signal is processed by the audio processor (described below), it is re-input to the analog interface, where it is converted to analog audio and output.

③Audio processor

This processor applies a variety of radio and audio processing to the digital signal input from the analog interface.

Radio processing includes the following algorithms: AM/FM noise reduction, AM/FM detection, FM stereo demodulation, FM diversity, RDS, and multi-pass noise reduction.

Audio processing includes the following algorithms: Vol. control, Tone control, CSII (circle surround II), and FixEQ.

The audio processor also includes a digital input, so that by connecting a CD player, for example, you can create a CD tuner system.

Next, we will take a closer look at each part.

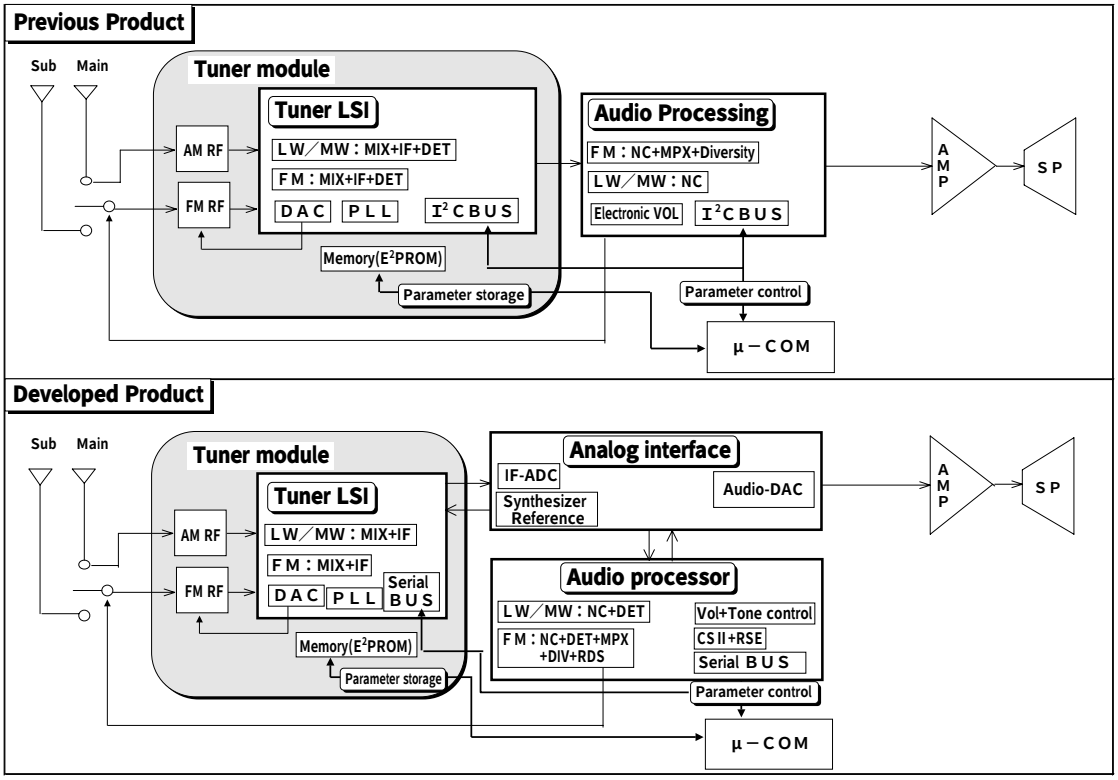


Fig.1 System block diagram (comparison with current product)

3.2 Tuner module

3.2.1 Tuner LSI

In conventional analog tuners, processing is performed by the front-end tuner LSI from the RF area to detection. However, since the tuner module we have developed performs digital processing after IF, no detection circuitry is needed. In addition, while a crystal oscillator is required in conventional tuners for the PLL reference frequency, in our newly developed system it is supplied from the analog interface. With these changes, the construction is simpler than conventional products.

Previous product

LW/MW: MIX + IF + DET
FM: MIX + IF + DET
Shared areas: PLL + DAC + BUS

Developed product

LW/MW: MIX + IF
FM: MIX + IF
Shared areas: PLL + DAC + BUS

3.2.2 Sliming of tuner module

Other companies have also been adding multiple functions to car audio devices over the years, resulting in large installation spaces. Our newly developed tuner needed to be 75% the height of the previous product. This sliming was achieved through a reduction in the functions of the tuner module, allowing the removal of several large parts and the use of compact parts.

Table 1 Tuner part composition

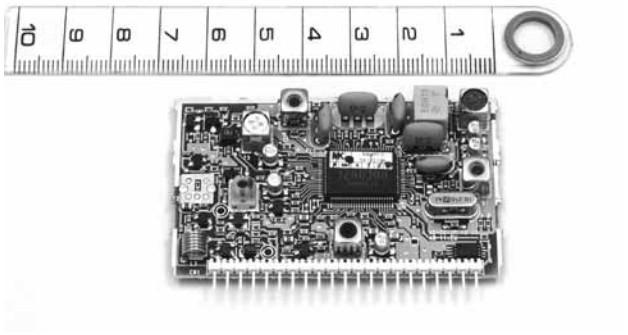
Item			Previous product	Developed product
Miniaturization	Height		40mm	30mm
	Area		10	8
Large parts	IC	Reflow	2	2
	Transformer, coil	DIP	8	4
		Reflow	0	2
	Filters	DIP	5	2
	Crystal oscillator	DIP	1	0

1005-size chip parts are not used in the previous product. However, they make up 40% of part in the developed product, and contribute to miniaturization. In addition, parts were successfully installed on one side, as with the previous product.

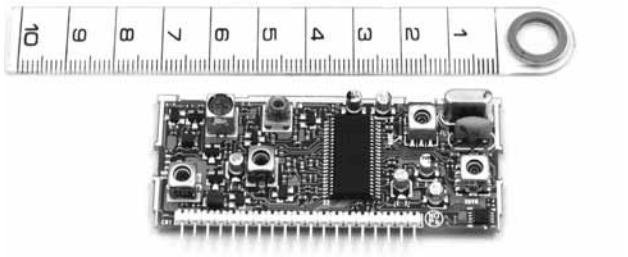
3.2.3 Improvements in productivity

As you can see in Table 1, although ALL reflow is not achieved through cost restrictions, DIP parts are reduced to 40% from the previous product (from 14 to 6), contributing to improvements in productivity and quality.

In addition, we are making rapid in-house progress for lead-free compatibility.



Previous product



Developed product

Fig.2 Outer shape comparison of developed and previous product

3.3 Analog interface

3.3.1 Process

A 0.35 (m 3.6 V standard CMOS process was used, based on considerations for analog signal processing such as AD/DA converters and analog volume control circuitry, the dynamic range of input signals, and power source voltage. The recommended operational voltage is the standard 3.3 V.

3.3.2 Block construction

An internal block of the analog interface is shown in Figure 3.

- **AD converter for IF signal input: differential input, 2 channels**
- **AD converter for stereo input: differential input, 2 channels**
- **AD converter for voice input: 3 channels**
- **Standard clock creation circuitry for LVDS interface**
- **Crystal oscillator circuitry: 28.8 MHz**
- **Serial protocol engine**
  Serial parallel interconversion of data, according to LVDS protocol
- **Data flow processor**
  Control of data transmission timing between internal blocks
- **Decimation filter for IF input**
- **Decimation filter for analog audio input**
- **Decimation filter for speech input**
- **Analog volume attenuator**
- **Audio DA converter: 6 channels**
- **Interpolation filter for audio output**
- **Control register**

After the intermediate frequency signal from the tuner module goes through AD conversion, the analog interface uses filters to convert the sample rate to the optimum value for processing by the base band chip in a later step. The AD converter for IF uses a ΣΔ AD converter with band-pass functionality to achieve an input dynamic range of approximately 80 dB at a transit bandwidth of ±140 kHz. A sampling frequency of 14.4 MHz is used, and the transit bandwidth is set to 280 kHz to avoid any effects due to aliasing noise. Sine the sampled IF signal becomes a 480 kHz signal when sent to the bass band chip in a later step, oversampling is performed 30 times. Two systems are included so that the AD converter is compatible with twin tuners. For external analog input, there are two systems for differential input stereo ADC, one system for differential monaural audio ADC, and two systems for single-end monaural audio ADC. Each of these can be used for cassette tape input, microphone input, intercom, external CD changer analog input, and auxiliary input. These analog signals input to the analog interface are processed by the audio processor in a later step, and then sent back to the audio interface, where they are converted to analog signals by the DA converter and output to the speaker amplifier. The DA converter has six channels, for L/R front, L/R rear, center, and sub woofer. The analog volume for varying the level of audio signal sent to the speakers can be varied in a 60 dB range in 1 dB steps, and is designed to prevent click noise (or pop noise) that can be produced when changing volume settings. LVDS (low voltage differential signal) is used for sending/receiving digital data between the audio processor and analog interface, as well as for supplying the standard clock, with consideration for suppressing the effects of radiation noise and common mode noise. Since the standard clock can be supplied for the tuner module PLL, there is no need to make a separate connection for a standard clock crystal oscillator in the tuner module. A function is included that turns off DAC and ADC blocks that are not actually used due to model specifications, to conserve power.

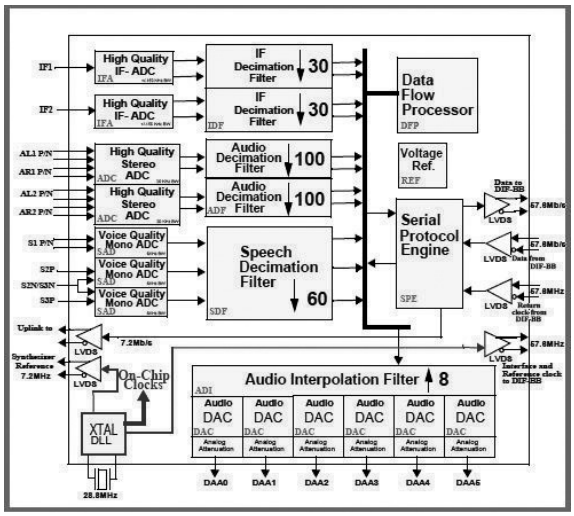


Fig.3 Internal block of analog interface

3.4 Explanation of audio processor

3.4.1 Process

Since improvements in digital processing capacity can be expected due to the shrinking of process through the use of a different chip than for the analog processing block, a minute CMOS processor with 0.18 (m TSMC is used. At a DSP core operation power supply voltage of 1.9 V, a maximum operating frequency of 160 MHz is achieved.

3.4.2 Block construction

An internal block of the audio processor is shown in Figure 4.

- **Main DSP core (Onyx)**
- **On chip memory**
- **Core processor (9):**
  DFP, RCB, DMD, UPS, CEP, VIFF, FIFF, ASRC, RDS_0-digital audio interface (SPDIF) receiver: (2 ports) compatible with IEC958, S/PDIF, CP-340, and AES/EBU digital audio formats
- **ESAI (Enhanced Serial Audio Interface): 2 blocks**
  Up to 4 ports for reception channels and 6 ports for transmission channels can be set for one ESAI.
- **GPIO: 8 channels**
  Two channels are set for diversity antenna change signal output.
- **Serial host interface:**
  Compatible with I2C and SPI, and 5 V and 3 V systems.
- **Watchdog timer**
- **PLL for internal clock creation**
- **LVDS interface**
- **Hardware for RDS reception**

DSP and each co-processor have a total of 1300MIPS of processing capacity (at 147 MHz operation). Post-acoustic processing and signal processing after radio demodulation are performed in the main DSP core (Onyx), and pre-modulation radio signal processing is performed mainly by the co-processors. The co-processors that perform radio signal processing (except for some) make up a block defined by the software, are handled as independent DSP, and included individual memory regions. In the digital audio input interface, there is an internal asynchronous sample rate converter that converts audio signals with different sample rates to a common sample rate. There are various libraries for use as post-audio processing functions, for parametric equalizer, graphic equalizer, audio spectrum analyzer, bass, treble, balance, fader, dynamic compression, loudness control (bass boost), CSII, beep, and mute. In addition, there is also a function for mixing audio signals from the external microphone input, such as from a navigation system. It can also be used as an audio decoder, with support for multi-channel decoding such as for Dolby digital from a DVD source and Dolby pro logic II. The bass band processor includes an AM/FM demodulation function, in addition to audio processing with a processor compatible with simultaneous dual source processing.

LVDS is used for transmission between the audio processor and the analog interface, with a high-speed transmission of 57.6 MBps for data transmission/reception between chips. The internal clock receives the standard clock (57.6 MHz) via LVDS from the external analog interface chip, creating the operating clock by decreasing the frequency with the DSP internal PLL.

Although the RDS (or RBDS) block for data broadcasts in Europe and North America support the decoding function, it is also possible to connect the demodulation output to an external decoder.

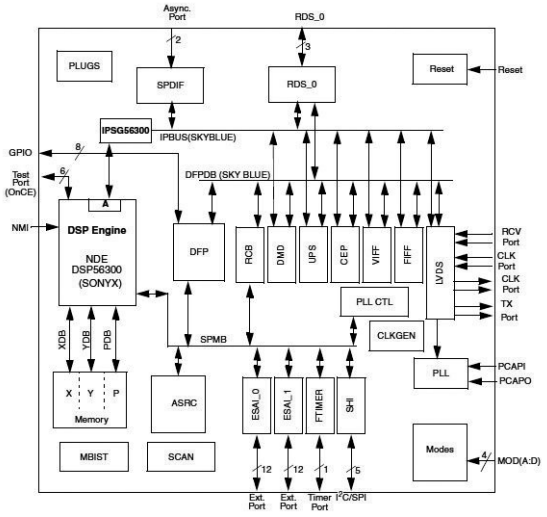


Fig.4 Internal block of audio processor

3.4.3 Main DSP internal memory

Y data RAM: 16k words
Y data ROM: 4k words
X data RAM: 16k words
X data ROM: 4k words
Program ROM: 20k words (internal boot ROM: 1k words)
Program RAM: 12k words
Y data RAM: 2k words
X data RAM: 2k words

4 Newly developed functions

This is our first digital signal processing tuner, with a variety of software algorithm developed with Freescale Semiconductor, Inc. to improve performance.

Following are descriptions of its most notable features.

4.1 Improvement in AM noise elimination

The main two goals in achieving digital processing for the AM noise canceller are as follows.

①Achieve a signal processing method that applies the merits of digital processing, to improve listening performance.

②Dramatic improvements in noise reduction over the previous product

A block diagram of the AM noise canceller developed for these goals is shown in Figure 5.

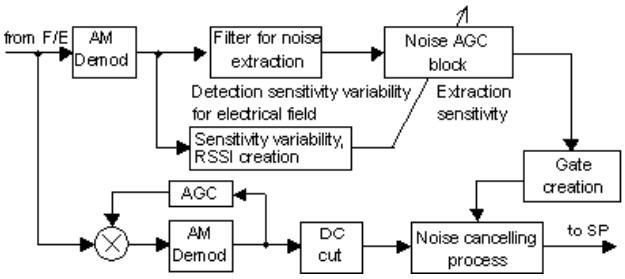


Fig.5 Block diagram of AM noise canceller

4.1.1 Improvement of listening performance

The extent to which noise production regions can be smoothed (interpolated) is important for listening performance during noise interpolation. With this interpolation method, we improved the reduction of distortion and listening performance during noise interpolation through the use of wave pattern prediction interpolation process that uses ADF (adaptive digital filter) that can predict the current wave pattern from the signal before noise was produced. The wave patterns during interpolation are shown in Figure 7. This shows that the noise interpolation area (shown by the dotted lines) is smoother than for the previous product.

Adaptive filters are filters with properties automatically determined by an input signal with that property. They are achieved by calculating the filter coefficient correction algorithm so that the square of the expected value of the error signal e(n) = x(n) - y(n), which is the difference between the input signal x(n) and the output signal y(n), is at its minimum value, and updating the variable filter. (Refer to Figure 6.) Although adaptive filters can be constructed from analog filters, the circuitry becomes large and impractical. Therefore, the use of this adaptive digital filter in the noise interpolation method is one big benefit in digital processing.

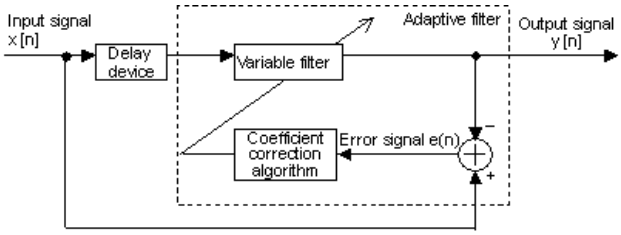


Fig.6 Block diagram of adaptive digital filter

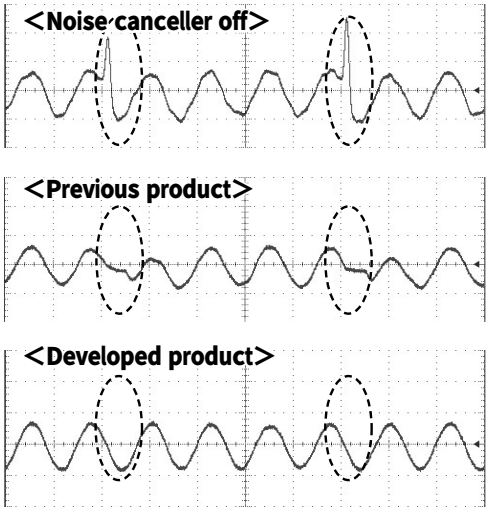


Fig.7 Comparison of interpolation wave patterns

4.1.2 Improvement of noise reduction performance

Noise reduction performance is determined by the noise detection area.

The circuitry in the noise detection area is made up of the following blocks:

- **the AM synchronous detection block for noise detection,**
- **the filter for extracting noise components from detected signals,**
- **the noise AGC block for preventing the malfunction of the noise canceller due to audio or white noise components,**
- **the block for creating electrical field strength (RSSI), and**
- **the block creating the gate for controlling noise canceling processes. (Refer to Figure 5.)**

A feature of the noise detection area is simultaneous malfunction due to noise detection features and audio, due to the changes caused by electrical field strength (RSSI) to the detection sensitivity determined by the noise AGC block. (Refer to Figure 8.)

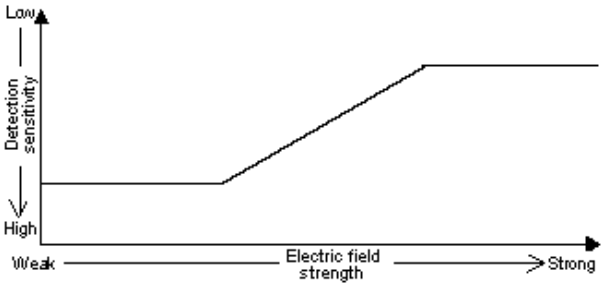


Fig.8 Level of detection sensitivity vs. electrical field strength

The noise elimination properties measured with the constructions and controls described above are shown in Figure 9. The symbols used in the Figure indicate the following:

- **S: Signal level**
- **N: Noise level**
- **P: Pulse noise level**

Both graphs show that noise elimination properties improve as the level difference between "S + N + P" and "N + P" increases. Even a comparison of an electric field strength of 50 dBuVemf, the worst N + P level for the developed product, shows an improvement of approximately 20 dB over the previous product.

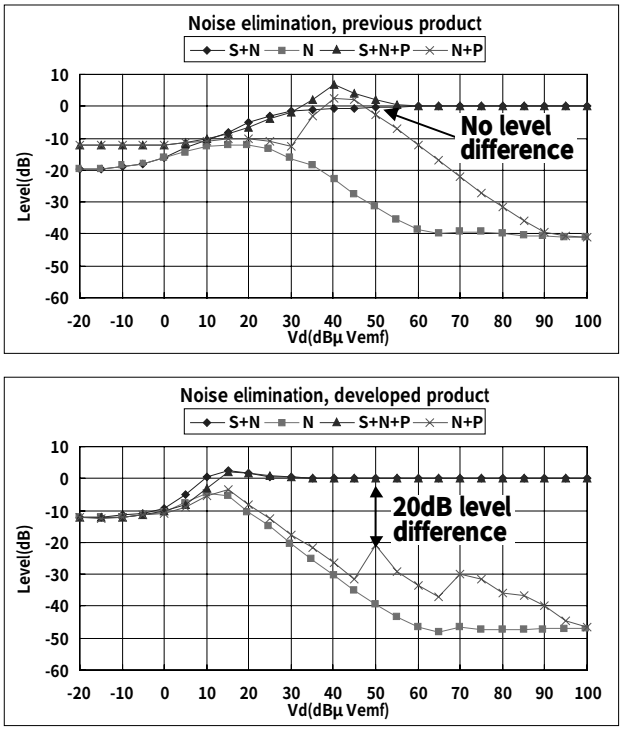


Fig.9 Comparison of noise elimination properties

4.2 Improvements in FM noise elimination

4.2.1 Single tuner diversity

Diversity is a function for selecting between two installed antennas for the one with the best signal quality, when multi-pass noise and poor electrical field conditions occur when trying to receive FM broadcasts while driving. The system for using a single tuner with a device for selecting antenna input, and selecting with the control signal from the diversity circuitry (single tuner diversity) has become mainstream due to its cost effectiveness.

We have developed a new algorithm for the single tuner diversity function through digital processing. As a result, the antenna with the better receiving conditions can be selected more quickly than with the diversity function in the analog circuitry of the previous product, and multi-pass noise is dramatically reduced.

A flow chart of the new sensitivity variability algorithm is shown in Figure 10. With the diversity used in previous analog circuitry, systems were constructed by combining functions that adjusted antenna adjustment sensitivity by the rate at which multi-pass noise occurred, with functions where antennas were fixed as the rate of antenna selection increased. Since performance has been improved with a simpler construction through digital processing, these systems were not simply replaced. Instead, we applied an algorithm that uses multi-pass detection and a counter for managing time to prevent excess antenna selection, while comparing the noise level between both antennas.

A comparison of diversity reception between the developed product and the previous product is shown in Figure 11 on the previous page. Since the developed product has a new sensitivity variability algorithm that sets the size of the multi-pass noise of the antenna before switching to the antenna switching threshold value after switching (Refer to Figure 10.), it is possible for B-ANT, with the better reception conditions, to be selected momentarily. However, with the previous product, since antenna switching threshold value was controlled by the rate of the occurrence of multi-pass noise, A-ANT may have been selected, resulting in poorer listening performance than for the developed product.

In addition, with a diversity system in which a switching device is placed at the antenna input, noise will be produced by antenna switching. Although this noise is produced across the entire electrical field and is very annoying, it can be eliminated somewhat with an FM noise canceller. However, with the previous product, there were limitations to noise detection devices, particularly for radio wave conditions in intermediate electrical fields or less, and it was impossible to completely eliminate the noise. With the developed product, the antenna

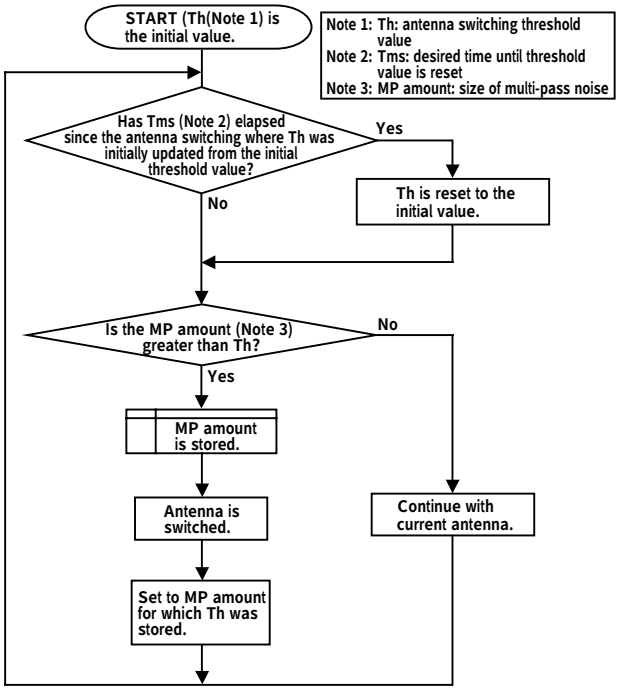


Fig.10 Outline flow chart for sensitivity variability of developed products

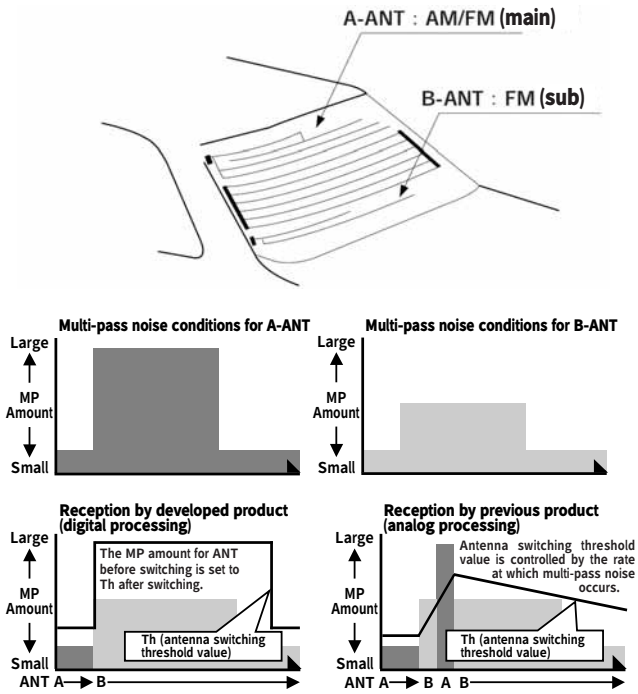


Fig.11 Diversity reception properties comparison between developed and previous products

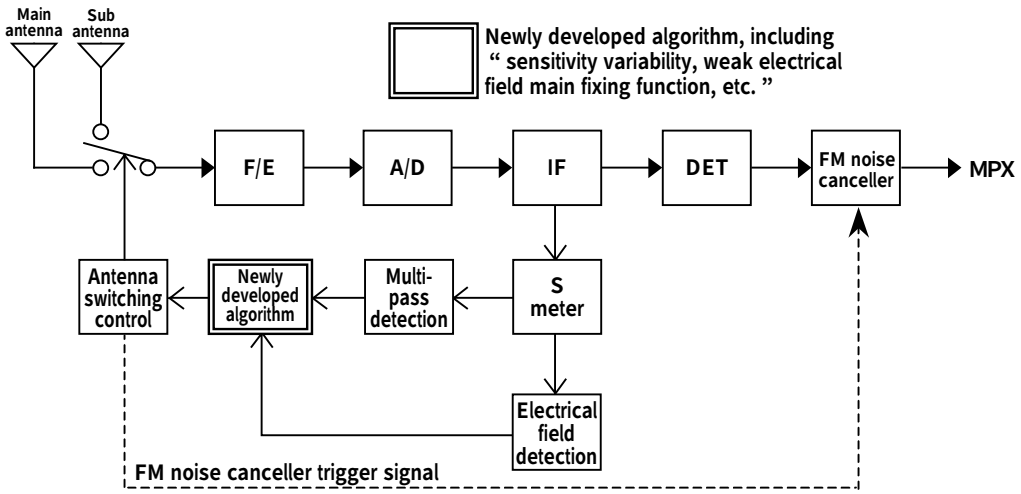


Fig.12 Block diagram of diversity

switching control signal is used as a trigger to operate the FM noise canceller (the dotted line in Figure 12 on the previous page), allowing the complete elimination of noise caused by antenna switching, and improving the listening performance when there is frequent switching of antennas.

4.2.2 Channel equalizer

(complex applied algorithm)

Although diversity systems are extremely effective in improving multi-pass performance, they require multiple antennas and are difficult to apply to all cars.

With the previous analog system, multi-pass noise in the L-R component could be reduced by reducing the amount of separation, and the high-pass noise of annoying frequencies could be reduced by changing the amount of high-cut.

In addition to these processes, an algorithm called a channel equalizer, which automatically corrects noise that occurs due to multi-pass, was used to improve multi-pass performance in the developed product.

Due to the propagation characteristics of FM waves, signals from multiple reflections caused by building and other obstacles are received by a single antenna. A phase difference is caused by the delay in these multiple signals, affecting the received signal. This block is a complex adaptive control FIR filter based on CMA (constant mod-

ulus algorithm), which operates blindly in response to the FM amplitude modulation component (blind algorithm).

In addition to the reduction of multi-pass noise, it also functions to reduce the effects due to group delay caused by external filters in the analog front end, and improves stereo separation. Multi-pass includes frequency-selective phasing, which generally occurs in various areas within the reception bandwidth, and flat phasing, which uniformly affects the entire reception bandwidth. The channel effect processor, due to its features, is optimized to be effective for frequency-selective phasing.

With the use of complex adaptive algorithms, we were able to reduce the rate of multi-pass noise when compared to previous analog processing.

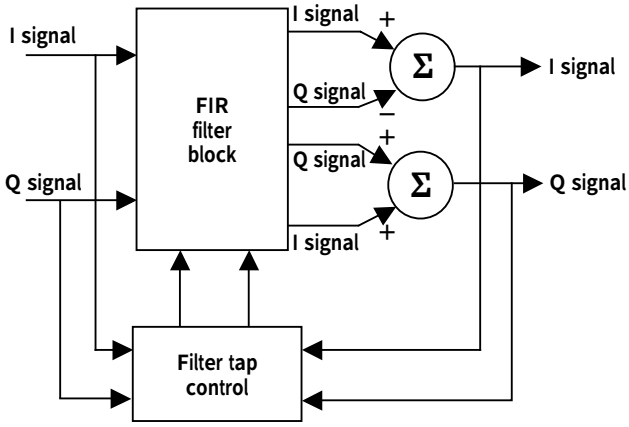


Fig.13 Channel equalizer

4.3 Improving the prevention of FM interference

(FM automatic variable bandwidth switching algorithm: VIFF)

The channel space for receiving FM broadcasts is 200 kHz in the US and Europe, and 100 kHz in Japan and Europe. Interference occurs in receivers when there is a broadcast station closer to the reception site than the desired broadcast station, and when the electrical field strength of the nearby broadcast station is strong. In response to this problem, a digital variable bandwidth IF filter (VIFF) has been used for electrical field strength variety of nearby broadcast stations to prevent interference. Normally for analog systems, several external ceramic filters are used to change between bandwidths. However, we have achieved the elimination of nearby interference that is superior to analog systems, and without the use of external ceramic filters. In addition, with digital filters, the bandwidth can be adjusted at a smaller frequency step (25 kHz, for example) than with ceramic filters. Since processes are performed automatically with the DSP algorithm without using the microcomputer or controls, load on the microcomputer is reduced, making this system optimal for reception while moving, when reception conditions are changing constantly. VIFF is set so that the bandwidth is controlled from 25 kHz to 100 kHz at steps of 25 kHz. If overmodulation occurs, the bandwidth is covered up to 150 kHz. (Up to 200% is allowed.) The specifications stipulate a sample rate of 480 kS/s, and an attenuation outside the bandwidth of 80 dB or greater. The system was designed with consideration for efficient combination of parts while maintaining performance with limited system resources using a complex filter with filter banks.

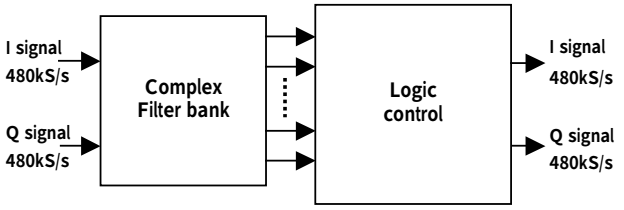


Fig.14 Automatic variable bandwidth switch algorithms

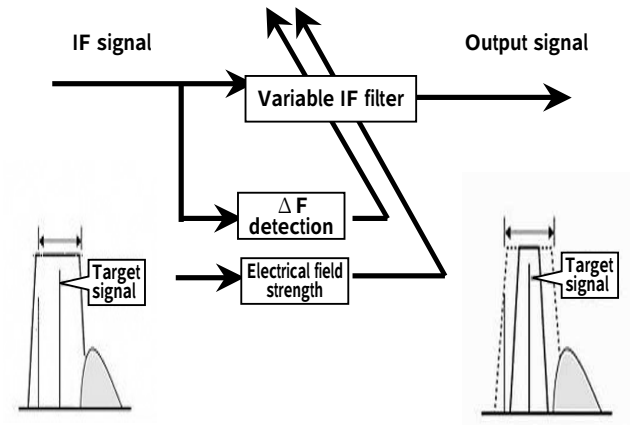


Fig.15 Image chart of automatic variable bandwidth switch effects

5 Results of developed product

As explained above, we were able to achieve performance as good as or better than analog tuners, at a size and cost equal to or less than for the previous product.

The main printed boards are shown installed for the developed product and the previous product in Figure 15. The tuner module and DSP (including audio processing area) are enclosed by a black line.

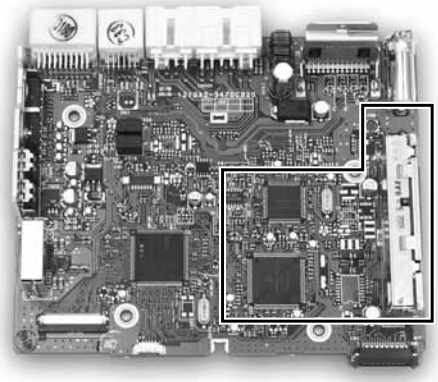
To achieve the size and cost performance of the developed product while retaining the structure of the

Item	Performance		Size	Cost
	Noise elimination	Adjacent		
Developed product	◎	◎	○	○
Previous product	○	○	○	○

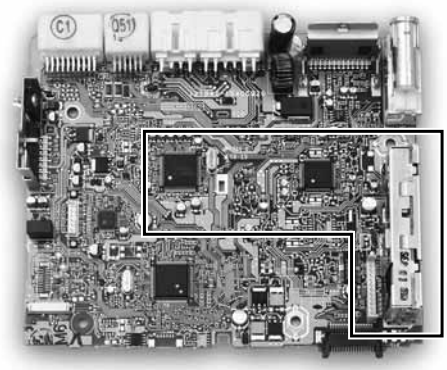
○ : Equivalent or better
◎ : Excellent

Fig.16 Effects of development

previous product (analog circuitry), additional AMPNR circuitry would be required, resulting in a product that is larger and more expensive than the developed product.



Main printed board installed with developed products



Main printed board installed with previous products

Fig.17 Comparison of main printed boards installed with developed and previous products

6 Conclusion

With the development of a digital signal processing tuner, we were able to achieve the target radio performance, while also achieving DSP standardization with audio processing, such as sound field control, in the first step toward the standardization of process for other digital media.

In the future, we plan to further improve radio performance and standardize other digital media.

Finally, we would like to express our sincere gratitude to the people at other companies who assisted in the development of this system, as well as personnel in related departments within or own company.

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